Thermal Modeling and Performance of High Heat Flux SOP Packages

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***Abstract*—This paper explores the thermal challenges in advanced system-on-package (SOP) electronic structures, as well as candidate thermal solutions for these highly demanding cooling needs. The heat fluxes on the active surfaces are expected to approach 100 W/cm^2. The impact of this high flux is exacerbated by the relatively low thermal conductivity of the organic materials in SOP packaging. Detailed three-dimensional (3-D) finite-element simulations were used to study the temperature distributions in a typical SOP package, and to provide guidance for the development and implementation of "compact thermal models". These models were used to evaluate and compare the performance of various thermal technologies and to establish the most promising thermal management alternatives. The use of direct liquid cooling, by immersion of the components in inert, nontoxic, high dielectric strength perfluorocarbon liquids was seen to provide effective cooling over a range of anticipated SOP power dissipations.**

***Index Terms*—Compact model, finite element method, high flux, liquid cooling, system-on-package (SOP).**

I. Introduction

TECHNOLOGICAL advances in the microelectronics industry have led to a rapid increase in the transistor density and speed of electronic chips, which resulted in increase in the dissipated heat flux. Based on the International Technology Roadmap for Semiconductors (ITRS Report, [19]), total power consumption continues to increase due to the higher chip operating frequencies, the higher interconnect overall capacitance and resistance, as well as the increasing gate leakage of exponentially growing and scaled on chip transistors. The expected chip heat fluxes are expected in excess of 70 W/cm^2 by end of this decade, and about 100 W/cm^2 by 2018.

The "System-on-Package," or SOP, is a fundamentally new microelectronics paradigm, which is expected to drive microelectronic system design in the 21st century. While the invention of the transistor revolutionized every aspect of electronic products, passive components, including resistors, capacitors, inductors and piezoelectric components, are today an important roadblock to the further miniaturization of many electronic products. The SOP technology integrates these passive elements directly into/onto the SOP substrate while at the same time maintaining the low cost nature of the process. The SOP integration and mounting of the chips over the low profile, thin film passive devices, yields several benefits including reduction in board size by as much as 80%, and improvement in reliability and cost.

Due to the high level of integration of SOP electronics, the heat flux on the active surfaces is expected to approach 100 W/cm^2. The impact of this high flux is exacerbated by the relatively low thermal conductivity of the organic materials, which can lead to relatively large temperature gradients between components populating the substrate. Consequently, thermal management of SOP packages requires detailed thermal models, and the application of aggressive cooling techniques for the active components.

At a typical allowable temperature difference of 60 K, between the component surface and the ambient, "natural" cooling in air, relying on both free convection and radiation, is effective only at heat fluxes below 0.05 W/cm^2. Thus, a very large heat sink or an unacceptably large chip-to-ambient temperature difference would be needed to provide high heat flux cooling. Although forced convection cooling in air offers approximately an order of magnitude improvement in the heat transfer coefficient, this thermal configuration is unlikely to provide a heat removal capability in excess of 1 W/cm^2 even at an allowable temperature difference of 100 K. Consequently, to facilitate the transfer of moderate and high heat fluxes from component surfaces, the thermal designer must choose between the use of finned, air-cooled heat sinks and direct or indirect liquid cooling. Finned arrays are sophisticated techniques for improving convective heat transfer coefficients and can extend the effectiveness of air cooling to progressively higher component heat fluxes but often at ever increasing weight, cost, and volume penalties.

When package heat fluxes approach or exceed 10 W/cm^2, attention must be turned to nonconventional cooling techniques. Most existing liquid cooling designs involve heat transfer by conduction across a lightly loaded interface between the package and a heat sink, followed by convection from the heat sink to that coolant. In such schemes, the thermal contact resistance between the surface and the heat sink often limits the maximum heat flux removable from the active surface at a given surface temperature. This resistance can be eliminated by immersing the package in 3M's perfluorinated liquids [31], which provide high dielectric strength, a low dielectric constant, and chemical inertness. Consequently, many observers believe that direct immersion cooling, using such dielectric liquids, could become the method of choice for thermal management of advanced electronic systems (Bar-Cohen, [5]), and thus remove component heat fluxes of the order of 50 W/cm^2 with saturated pool boiling at temperature differences typically less than 20 K.

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TABLE I
COOLING SCHEMES AND CORRESPONDING HEAT TRANSFER COEFFICIENTS. (BAR-COHEN *et al.* [6])

Cooling Scheme	h [W/m^2-K]
Natural convection — Air	5
Forced convection — Air	50
Jet impingement with heat sink — Air	200
Forced convection — FC-72	1000
Nucleate boiling — FC-72	2000
Spray cooling — FC-72	3000

TABLE II
DIMENSIONS AND MATERIAL PROPERTIES OF THE HIGH-HEAT DENSITY SOP PROTOTYPE

Component	Dimensions [mm]	k [W/m-K]
Large die	20 x 20 x 0.3	148
Each small die	6.6 x 6.6 x 0.3	148
Interconnect layer	0.3	1-300
Underfill thickness	0.1	1
Substrate	46 x 23 x 6	1-300

II. THERMAL MANAGEMENT TECHNIQUES

From air cooling to high performance liquid cooling, passive to forced convection, single phase to two phase flow, thermal design engineers have many choices to meet their design needs. However, at the very first stages of a thermal design most of the thermal management techniques are eliminated due to their cooling power, cost, or reliability reasons. Many techniques, from indirect cooling to direct liquid cooling, have been studied by researchers over the last three decades to meet the thermal needs of low to high flux electronics. Table I presents the baseline heat transfer coefficients for various cooling methods. These convective coefficients will later be used in the compact and detailed thermal models. This section will give a short overview of literature about various cooling schemes.

As part of an extended effort to define the limits of passive immersion cooling, Arik and Bar-Cohen [2] conducted an experimental study of ebullient cooling with the new dielectric liquids for a broad range of pressures and bulk temperatures. The highest passive pool boiling CHF values for both HFE-7100 and HFE-7200 were observed at elevated pressures (3 Bar), attaining values of 53 and 59 W/cm^2 respectively, at subcoolings of 80 K and 93 K, respectively, and demonstrated the potential to use microporous coatings to increase these values by some 50%. The development efforts of EDIFICE (Embedded Droplet Impingement For Integrated Cooling of Electronics), involving an integrated spray-cooling device microfabricated in silicon, being developed for package-level cooling of high-heat flux electronics, were summarized by Murthy *et al.* [24]. The EDIFICE projects is aimed at using droplet impingement-cooling to remove component heat fluxes in the range 50–100 W/cm^2 using 50–100-μm water droplets and surface texturing on the backside of the chip to promote spreading and boiling.

A cooling method, based upon vibration-induced droplet atomization (VIDA), which can generate small liquid droplets and propel them onto a chip surface, was developed by Heffington *et al.* [16]. The VIDA technique involves the violent break-up of a liquid film into a shower of droplets by vibrating a piezoelectric actuator and accelerating the liquid film at resonant conditions. Initial heat transfer results, utilizing water and a simple cell design, have shown that the VIDA process can achieve cooling rates of over 100 W/cm^2. Later, Heffington *et al.* [17] reported heat fluxes as high as 200 W/cm^2, when a chilled water heat exchanger was used as the external heat removal device.

Bash *et al.* [8] introduced a unique thermal management architecture that employs vapor-compression refrigeration to cool multiple independently operating microprocessors in a small volume for high flux electronics. The refrigeration system was driven by a novel acoustic compressor that was variable speed, oil-less, and orientation independent so that it could operate under various operating conditions. A prototype 5 U server with four 100 W processors was built, and experimental results were presented and indicated that the innovative compressor technology can meet the thermal needs by keeping the chips below junction temperature.

A study of pool boiling at atmospheric pressure from single-layered, microchannel enhanced structures was presented by Ghui and Joshi [15] for a dielectric liquid (PF5060). The en-

TABLE III
EFFECTIVE PERPENDICULAR THERMAL CONDUCTIVITY

Parameter	Expression	Value
L_{via}	Length of Via	624 [μm]
$t_{interconnect}$	Thickness of interconnect layer	0.3 [mm]
$A_{dielectric}$	Area of the dielectric	9.33×10^{-7} [m^2]
$R_{\perp via}$	$1/(k_{copperLvia})\Sigma(\Delta x_i/w_i)$	143 [K/W]
$R_{\perp dielectric}$	$t_{interconnect}/(k_{dielectric}A_{dielectric})$	321.5 [K/W]
$R_{\perp unitcell}$	$R_{\perp via} \parallel R_{\perp dielectric}$	99 [K/W]
$k_{\perp}$	$t_{interconnect}/(R_{\perp unitcell}A_{dielectric})$	2.3 [W/m-K]

hanced 1 mm thick structures were fabricated in copper with an overall size of 10 mm × 10 mm. Parallel microchannels were cut on the bottom surface, and parallel microchannels at the top surface aligned 90° to those on the bottom surface. The structures were included in a natural circulation flow loop, consisting of an evaporator section, connecting tubes and a condenser. The enhanced structures were found to be highly efficient in promoting boiling heat transfer at the low heat fluxes ($q < 8$ W/cm^2) and to achieve a peak heat flux of 59.6 W/cm^2 at a modest superheat of 29.2 K.

Another interesting study by Zhang *et al.* [30] was presented on thin film based SiGe superlattice microrefrigerators for the removal of locally-high heat fluxes. Using fabricated and characterized micro solid-state refrigerators, they were able to demonstrate a localized cooling power density exceeding 500 W/cm^2, and a fast, 40 μs transient response of the SiGe/Si superlattice microrefrigerators. Faulkner *et al.* [14] reported on a study aimed at design solutions for heat fluxes exceeding 1000 W/cm^2. A test module, employing subcooled as well as saturated forced convection boiling heat transfer of water in a parallel micro channel heat sink, was designed and built. The working fluids tested included pure water and a selection of ceramic-based nanoparticle, water-based suspensions (nanofluids). Flow boiling with water was found to provide a 125-W/cm^2 capability for saturated boiling and 280 W/cm^2 for subcooled (25 °C) boiling, while the flow of nanoparticle suspensions was observed to dissipate heat fluxes in excess of 275 W/cm^2 at the substrate, while maintaining the substrate at or below 125 °C.

An experimental study of parallel and crosslinked microchannel heat sinks, with two-phase convective heat transfer of water, was presented by Cho *et al.* [11]. Due to the differences in the internal flow patterns, the crosslinked microchannel heat sink showed better cooling performance for localized (1-D) hotspots while the parallel microchannel heat sink displayed superior performance for extended (2-D) hotspots, at flux levels approaching 100 W/cm^2.

Due to the thermophysical properties water can enable higher heat removal capability. However, due to the high-hermal interface resistance, between the water-cooled cold plates and the microelectronic devices, water cooling systems are performance limited. Therefore, dielectric liquid cooling should be the first choice for high flux cooling. The superlattice approach can be used for spot cooling, but not for a large high flux thermal management application. Passive cooling such as pool boiling, perhaps, should be the first choice until it reaches its upper limits (∼80 W/cm^2), while spray cooling might be utilized for higher heat fluxes exceeding pool boiling limits. In the following section, thermal management needs of a typical SOP configuration

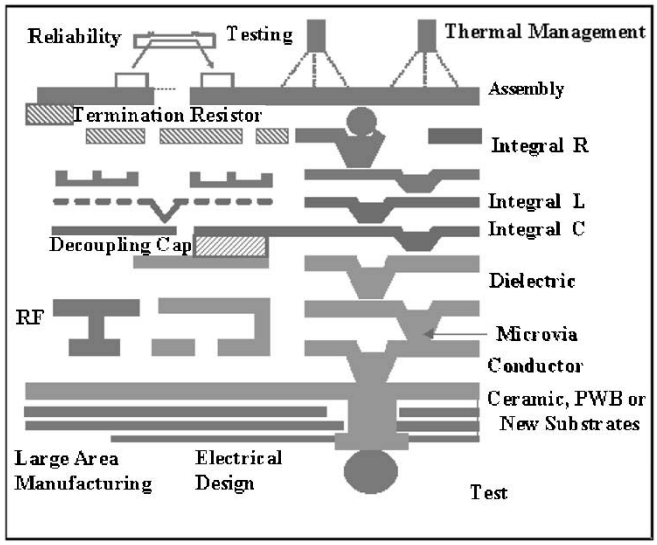

Fig. 1. SOP structure.

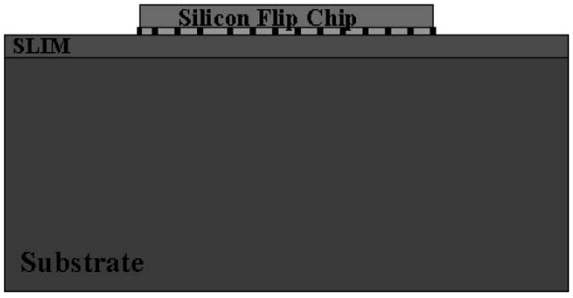

Fig. 2. Idealized SOP model.

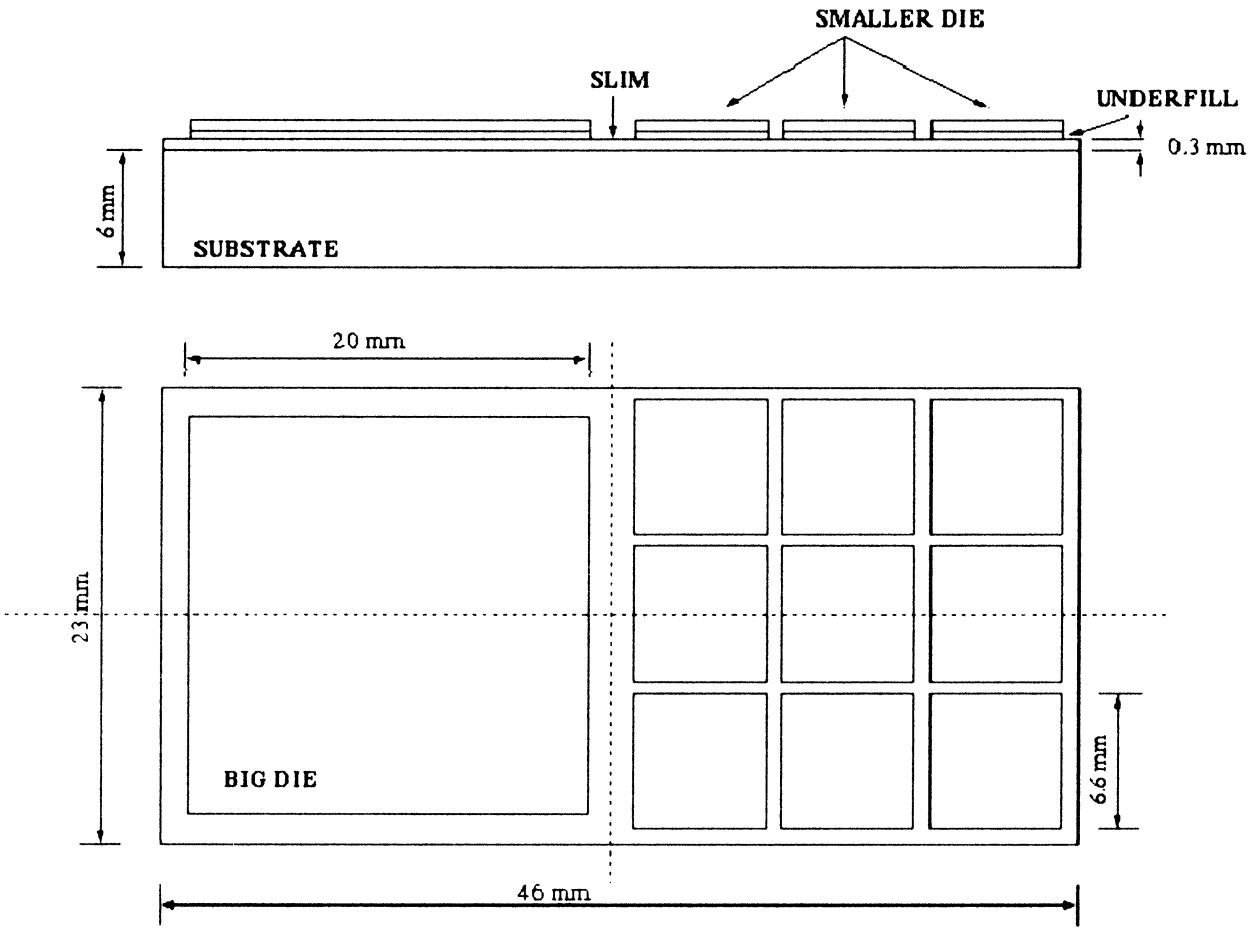

Fig. 3. High heat density MCM prototype.

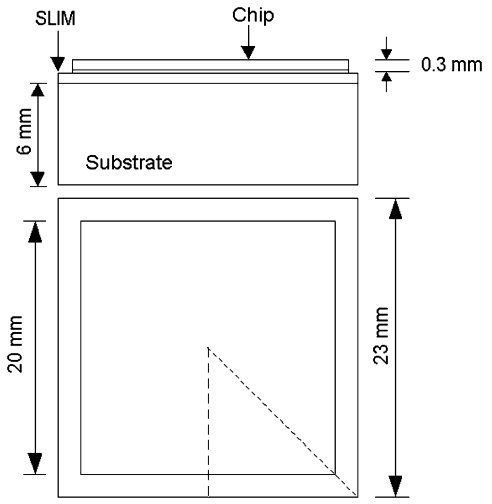

Fig. 4. Single-chip module.

and thermal performance will be outlined for various promising cooling techniques.

III. High Heat Density "System on Package" Prototype

Fig. 1 shows a typical SOP structure (Davis *et al.* [13]) and Fig. 2 shows the general arrangement of the components in a prototype SOP. In this packaging configuration, flip chips are mounted on top of the 300-μm-thick flexible interconnect layer by means of solder bumps and under-fill. All the passive components like resistors, inductors, capacitors, optoelectronics,etc. are integrated in this 300-μm-thick interconnect layer. The electrical connections between the various components and also the input/output for the chip are provided by means of copper vias in the layer, which is, in turn, supported on a 6-mm-thick organic substrate.

The roadmap for the thermal parameters are given in PRC Report [25]. Development of SOP was divided into three main phases. Each successive phase has higher packaging density and higher heat flux. The number of IO also increases in each successive phase. In the table the term silicon efficiency is defined as the ratio of the chip surface area to the substrate surface area. The chips are under-filled to decrease the thermal resistance and also to increase the reliability of the interconnect. In the last phase, heat flux dissipation is expected to reach as high as 100 W/cm^2. The maximum allowable temperature on the prototype is 95 °C. High heat flux dissipation makes it important to accurately predict the temperature profile and choose the proper cooling strategy to maintain the component temperatures below allowable limits.

All of the passive components, which are integrated into the interconnect layer, are connected to each other through copper vias. The complex geometry of vias makes it difficult to properly discretize the interconnect layer and generate the numerical

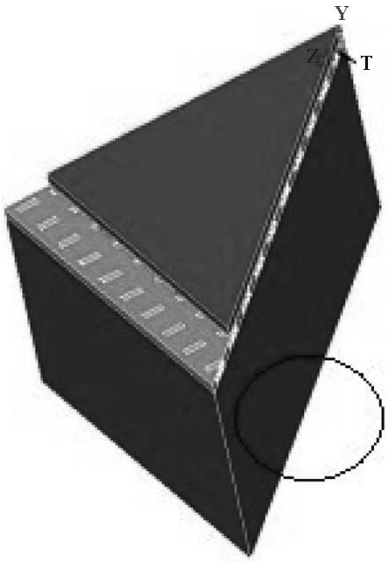

Fig. 5. Detailed model of single-chip module.

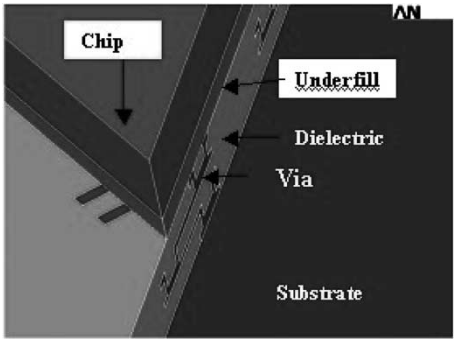

Fig. 6. Magnified view of single-chip module.

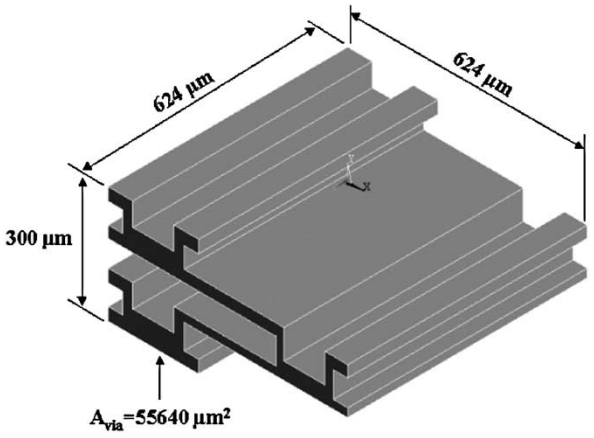

Fig. 7. Via geometry.

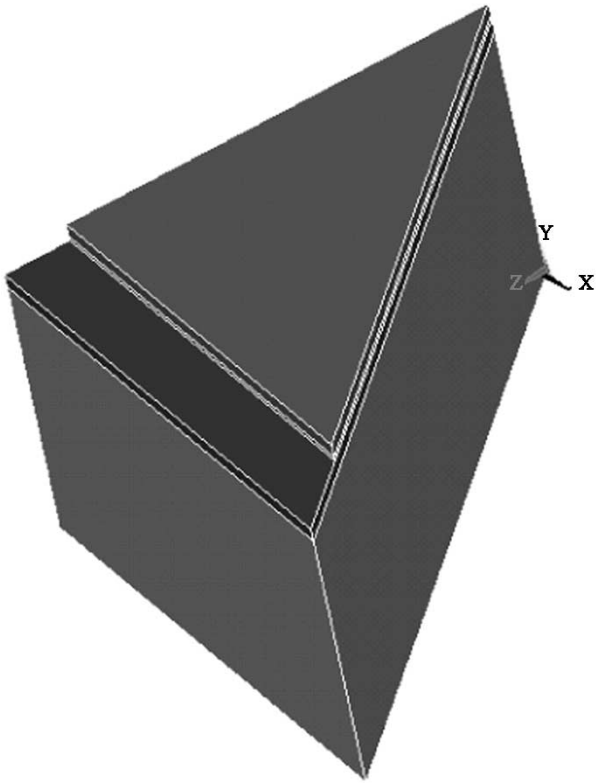

Fig. 8. Compact model (one-eighth symmetry).

model. The number of elements required to generate the mesh is large leading to a high computational time. Compact models for SOP prototypes were developed to reduce computational time. The compact model replaced the interconnect layer in the detailed model with a simplified representation that mimicked the behavior of the layer but had no vias in it. This compact model was achieved by using an analytically derived effective thermal conductivity, which took into account the presence of vias. The absence of vias in the compact model significantly simplified the numerical analysis. The number of elements required for the compact model mesh was 50% less than the detailed model.

As mentioned earlier, the high heat density SOP prototype is the thermally most challenging prototype. The compact model for the interconnect layer was derived in the context of this particular prototype. In other words, the agreement between the detailed model and the compact model was studied for the high heat density SOP prototype. Choice of the optimum cooling strategy that would allow the component temperature to be maintained below 95 °C, was also one of the aims of the study. Fig. 6 shows the details of the high heat density SOP prototype chosen for the thermal model. The total heat generation in the large chip is 80 W. The total heat generation for the nine smaller chips is also 80 W. The dimensions and material properties are summarized in Table II.

The effective thermal conductivity of the die-attach layer, including both the underfill and solder bumps, was set at 1.5 W/m-K, thus yielding a target $R_{die-attach}$, of 0.165 K/W. As the prototype is symmetrical an attempt was made to discretize the half symmetry model in the finite element code used for this study (ANSYS5.6, [1]). It was found that even at very low via density, the number of nodes required for meshing exceeded 128 000. To facilitate the modeling of as high a via density as possible in a commercial FEM code, the FEM model was separated into two parts; multichip module (i.e., MCM) and single-chip module and, as may be seen on Figs. 3 and 4 respectively.

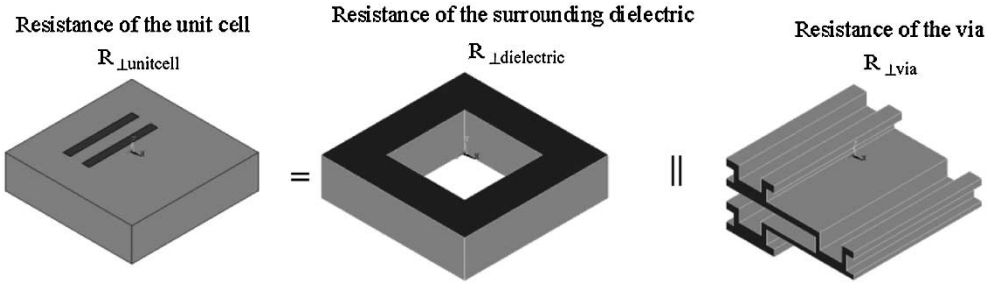

Fig. 9. Effective perpendicular resistance of the unit cell.

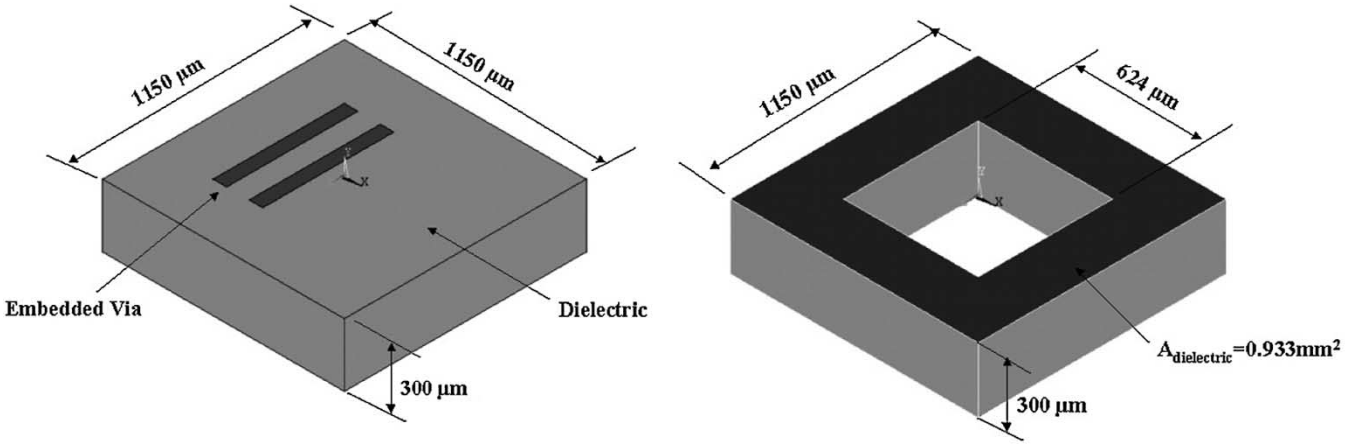

Fig. 10. Dimensions of the (a) Unit-cell (b) Surrounding dielectric.

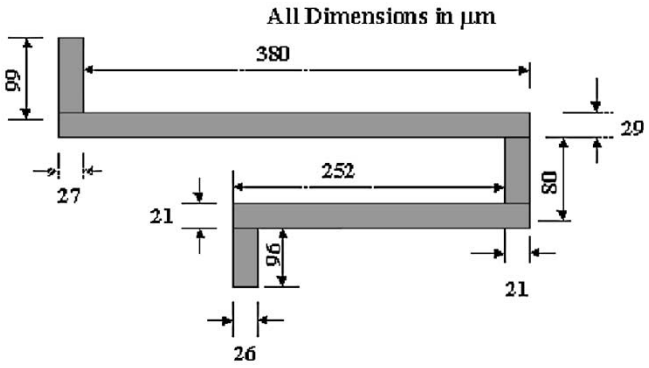

Fig. 11. Heat conduction path along the via.

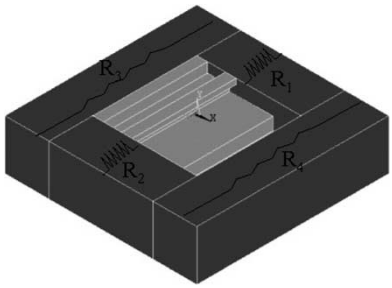

Fig. 12. Effective parallel thermal resistance.

IV. Finite Element Model of SOP Prototype

A. Single-Chip Module

1) Detailed Model: It can be seen from Fig. 4 that the module has one-eighth symmetry. Therefore to mesh the highest via density, only one-eighth of the module was discretized (marked in Fig. 4) in the finite element model (ANSYS5.6, [1]). Fig. 5 shows the detailed model for the single chip module. The one-eighth model allowed a via density of 75 vias/cm^2 to be meshed with 128 000 nodes.

The geometry of the vias embedded in the interconnect layer is shown in Fig. 7. The compact model was derived to make the thermal analysis of SOP prototypes more portable. Compact models required less memory space and less computational time for numerical analysis. The compact model replaced the interconnect layer in the detailed model with a simplified representation that mimicked the behavior of the layer but had no vias. This compact model was achieved by using an analytically derived effective thermal conductivity, which took into account the presence of vias in the interconnect layer. In order to validate the compact models, the temperature profiles obtained from the detailed numerical analysis were compared with those obtained from compact model numerical analysis over a wide range of parameters involved.

2) Compact Model: The compact model for the single chip module is shown in Fig. 8. The chip, the underfill layer and the substrate are modeled identically as in Fig. 5. The difference is in the modeling of the interconnect layer. The interconnect layer has vias in the detailed model, while in the compact model the interconnect layer is replaced by a homogeneous layer without any vias. The methodology adopted to derive the effective thermal conductivity assigned to the homogeneous layer in the compact model is presented below. The values

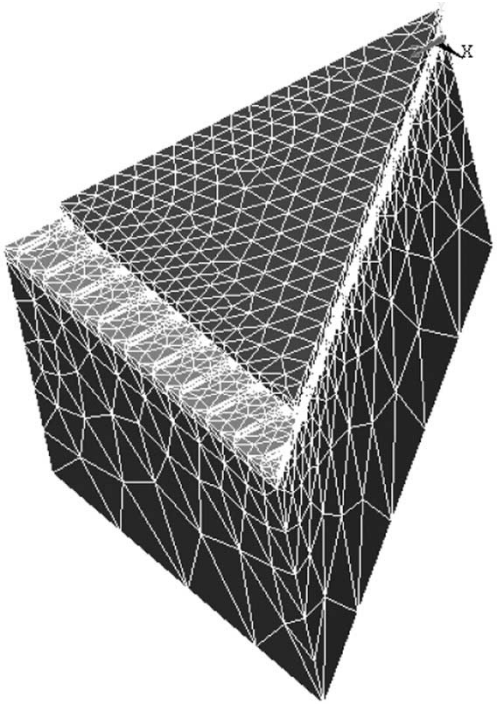

Fig. 13. Detailed finite element model.

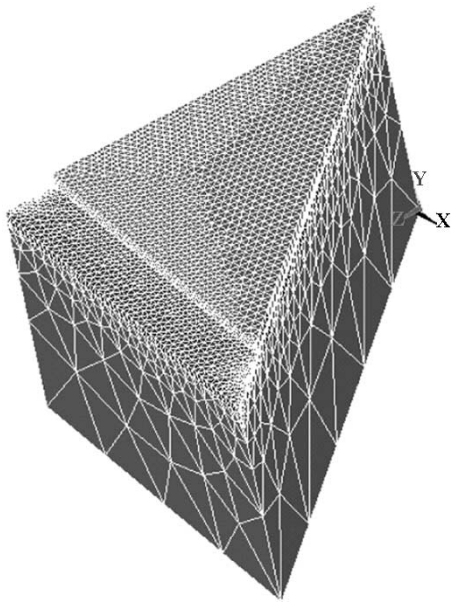

Fig. 14. Compact finite element model.

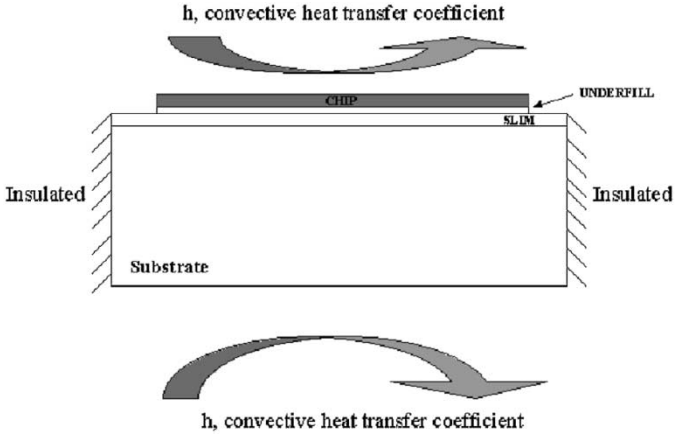

Fig. 15. Boundary conditions for single-chip module.

involved are for the specific geometry and materials that constitute this prototype. But the methodology adopted can be applied to prototypes of different dimensions and material compositions as well.

Effective Perpendicular Thermal Conductivity: The SOP unit-cell is shown in Fig. 10. The perpendicular conductivity of the unit-cell can be computed by obtaining the effective perpendicular thermal resistance of the unit-cell. As the thermal conductivity of copper vias is much higher than the thermal conductivity of the dielectric, heat conduction through the dielectric in between the via layers can be ignored. The effective thermal resistance is then the parallel combination of the thermal resistance of the via $(\mathrm{R}_{\perp \mathrm{via}})$ and the surrounding dielectric $(\mathrm{R}_{\perp \mathrm{dielectric}})$ as shown in Fig. 9. The thermal resistance of the via $(\mathrm{R}_{\perp \mathrm{via}})$ was derived by simply summing up the resistances of the individual segments along the heat conduction path in the via shown in Fig. 11. The dimensions of the individual segments along the via geometry are shown in Fig. 11. The values of the various parameters involved, various resistances and the effective perpendicular thermal conductivity are mentioned in Table IV.

3) Effective Parallel Thermal Conductivity: The heat conduction through the dielectric embedded in between the via layers was ignored again for the effective parallel thermal conductivity. The parallel thermal conductivity was obtained by determining the parallel resistance of the via $(\mathrm{R}_{\|\mathrm{via}})$ and taking it in combination with the resistance of the surrounding dielectric. Thus the effective thermal conductivities applied to the homogeneous layer in the compact model were 2.3 W/m-K and 1.6 W/m-K for perpendicular and parallel conductivities respectively.

A 10 node tetrahedral quadratic element was used for the discretization of numerical models. Figs. 13 and 14 show the finite element model for the detailed model and the compact model, respectively. The detailed model needed 87 743 elements while compact model needed only 31 885. In both the figures, the chip, the underfill and the substrate layers have been modeled identically. The difference between the two figures is in the modeling of the interconnect layer. In Fig. 13, the interconnect layer has been modeled with the copper vias in it. In Fig. 14, the interconnect layer was modeled without vias, but has an effective thermal conductivity applied, which takes copper vias into account.

Various boundary conditions were applied on the FEM model. The same boundary conditions were applied for both detailed and compact models. The sides of the module were assumed to be thermally insulated. A zero heat flux boundary condition was imposed upon the side surfaces as shown in Fig. 15. A convective heat transfer coefficient was applied on the top and the bottom surfaces of the module. The range of heat transfer coefficients studied in the parametric run was 5 W/m ^{2}-K representing natural convection air cooling to 3000 W/m ^{2}-K associated with pool boiling or spray cooling

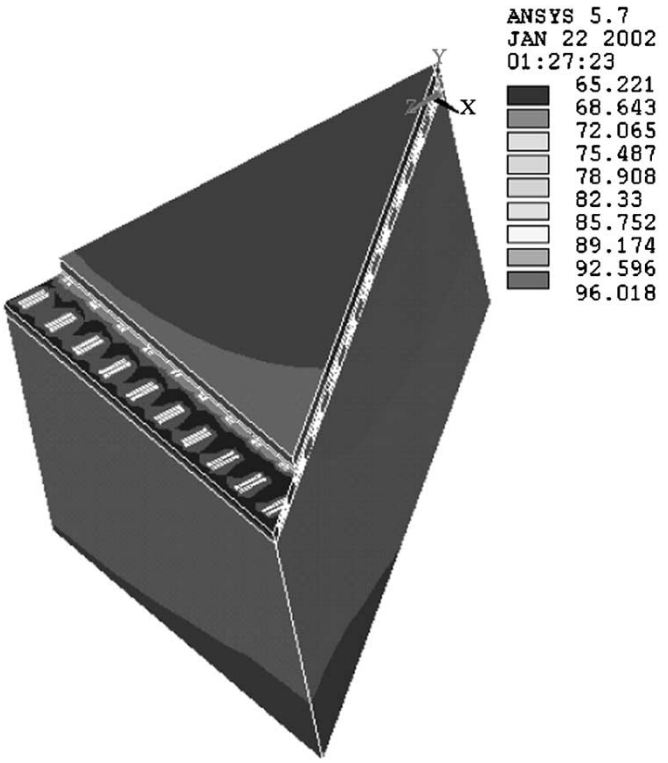

Fig. 16. Temperature profile of single-chip module (detailed model).

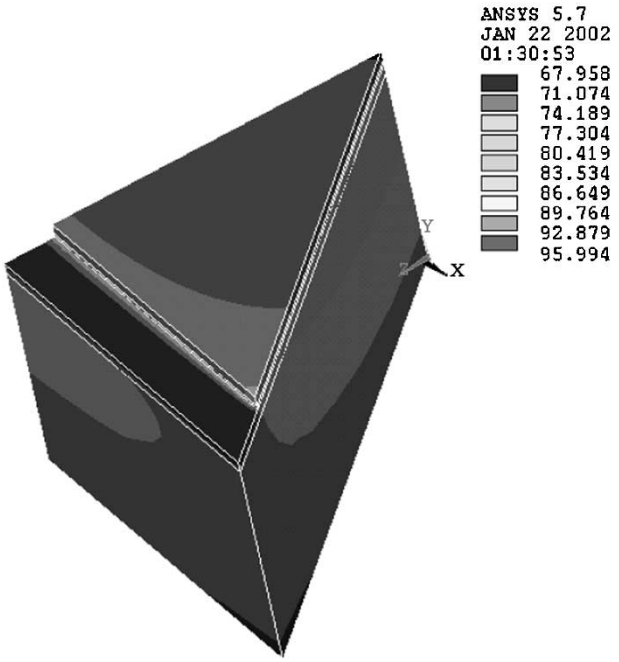

Fig. 17. Temperature profile of single-chip module (compact model).

with dielectric liquids. The ambient temperature was 45 °C for air-cooling, and 56 °C for liquid cooling. A volumetric heat generation was applied on the chip. The volumetric heat generation was calculated based on a surface heat flux of 20 W/cm^2. Volumetric heat generation was found to be 666.7 W/cm^3 Figs. 16 and 17 show the temperature profiles in the detailed and compact models for the case where the substrate thermal conductivity was set to 50 W/m-K and the heat transfer coefficient was set to 3000 W/m ^{2}-K. It can be seen that he application of same boundary conditions on the two models results in similar temperature profiles. A more detailed comparison of temperature profiles is discussed next.

The temperature profiles for the two models can be more directly compared using isotherms. The comparison is shown in Fig. 18.

As the heat transfer is in the boiling regime for the case shown in Figs. 16 and 17, the ambient temperature was set to 56 °C. The percentage difference between the two models was calculated using the following expression:

$$\text{Difference}[\%] = \frac{\text{T}_{\text{detailed}} - \text{T}_{\text{effective}}}{\text{T}_{\text{detailed}} - \text{T}_{\text{ambient}}} \times 100. \qquad (1)$$

The percentage difference between the maximum temperatures for the two models was 0.06%. In order to investigate if this agreement would hold over a wide range of heat transfer coefficient and substrate thermal conductivity, a parametric study was conducted for both the models and the maximum temperature comparison was made. A range of substrate conductivities was studied to go from organic low copper laminated structures to ceramic and silicon or even SiC and AlN. Between compact and detailed models, maximum and average chip temperatures,

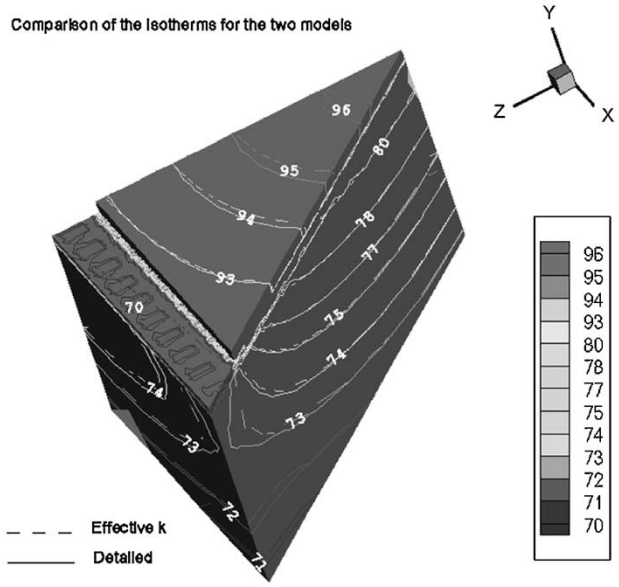

Fig. 18. Isotherms in detailed and effective thermal conductivity models.

average underfill temperatures, average interconnect temperatures and average substrate temperatures were given in tabular form. These comparisons have been presented in Tables V–IX. The detailed model results are in normal font and the effective-k model results are in bold font.

The maximum difference between compact and detailed models was also determined for SOP structure. The maximum difference between compact and detailed models was found to be 10% in the prediction of average underfill temperature. The compact model was able to predict the maximum chip temperature with a difference of 1.16%, and 3% for the substrate temperature respectively.

TABLE IV
EFFECTIVE PARALLEL THERMAL CONDUCTIVITY

Parameter	Expression	Value
$L_{unitcell}$	Length of the unit cell	1150μm
L_{via}	Via Length	624μm
A_{via}	Front area of the via	5.565×10^{-8} m^2
$R_{\|via}$	$L_{via}/(k_{copper} A_{via})$	28 K/W
R1 (=R2)	Dielectric Resistance (Fig 14)	1404 K/W
R3 (=R4)	Dielectric Resistance (Fig 14)	14580 K/W
$R_{\|unitcell}$	$(R_{\|via} + R_1 + R_2) \| (R_3 \| R_4)$	2027.5 K/W
$k_{\|}$	$1/(R_{\|unitcell} t_{interconnect})$	1.6 W/m-K

TABLE V
MAXIMUM TEMPERATURE FOR SINGLE CHIP MODULE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	592 594	481 481	433 433	431 431	429 429	427 427	Air Jet Impingement
2000	142 143	129 129	110 110	109 109	108 108	107 107	FC Nucleate Boiling
3000	116 116	109 109	96 96	95 95	94 94	93 93	Spray Cooling Nucleate Boiling

TABLE VI
AVERAGE CHIP TEMPERATURE FOR SINGLE CHIP MODULE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	577 580	471 471	430 430	428 428	427 427	425 425	Air Jet Impingement
2000	136 136	123 123	108 108	106 106	106 106	105 105	FC Nucleate Boiling
3000	111 112	104 104	94 94	93 93	93 93	92 92	Spray Cooling Nucleate Boiling

TABLE VII
AVERAGE UNDERFILL TEMPERATURE FOR SINGLE CHIP MODULE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	568 576	462 467	421 425	420 424	419 423	417 421	Air Jet Impingement
2000	132 135	118 121	102 105	100 104	100 103	98 102	FC Nucleate Boiling
3000	109 111	100 103	88 91	87 90	87 90	86 89	Spray Cooling Nucleate Boiling

B. Multichip Module

Large area die prototype analysis was divided into two parts as large chip and small chips sections. The analysis was performed for the one eight of the small chips section of the module (see Fig. 3). The temperature profiles for the multi chip module for one set of boundary conditions are shown in Figs. 19–21.

The substrate thermal conductivity was set to 50 W/m-K and heat transfer coefficient was set to 3000 W/m ^{2}-K. Again it can be seen that the application of same set of boundary conditions leads to similar temperature profiles.

The percentage difference between the maximum temperatures was found to be 0.09%. A parametric comparison of the different temperatures for the two models is presented in Tables X—XIV. Thus, for the multichip module, the maximum percentage difference was 12.9% for the average substrate temperature. The maximum percentage difference between the detailed model and compact model maximum temperature was less than 2% for both the cases studied (single-chip module,

TABLE VIII
AVERAGE INTERCONNECT LAYER TEMPERATURE FOR SINGLE CHIP MODULE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	536 523	443 438	409 409	407 407	407 407	405 406	Air Jet Impingement
2000	120 115	108 105	92 92	91 91	90 91	89 90	FC Nucleate Boiling
3000	100 96	92 90	80 80	79 79	79 79	77 78	Spray Cooling Nucleate Boiling

TABLE IX
AVERAGE SUBSTRATE TEMPERATURE FOR SINGLE CHIP MODULE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	498 510	429 432	404 404	403 403	403 403	402 402	Air Jet Impingement
2000	112 114	102 103	89 89	88 88	87 87	86 86	FC Nucleate Boiling
3000	94 95	87 88	77 77	76 76	76 76	75 75	Spray Cooling Nucleate Boiling

multichip module). The maximum percentage difference overall was 13% for the average substrate temperature. The compact model offers many advantages over the detailed model. Generation of the compact model requires much less effort as compared to the generation of the detailed model. The number of elements required for the mesh generation of compact model was almost one-third of the number of elements required for meshing of detailed model for the single chip module. Also because of the simpler geometries involved in the compact model, fewer elements have extreme shapes, reducing the numerical error involved in the simulations. The memory size of the temporary files generated during the simulations and also that of the final solution file is much smaller for the compact model. Total memory required for detailed model solution is 204 MB while compact model only needs 59 MB. It can be seen that the memory size of compact model solution file is less than one-third of the memory size of the detailed model solution file. The CPU time involved in the generation of the compact model is much less. The CPU time involved and the memory size of the files generated both during the generation of the model and the solution, made it nearly impossible to conduct the analysis of the detailed model on an *SGI Origin 200* server with two 180 MHz IP27 processors. The analysis was carried out on an IBM Supercomputer at the University of Minnesota-Supercomputing Institute. The compact model analysis however could easily be carried out on an SGI Origin 200 server. Thus compact model made the thermal analysis of the SOP prototype portable.

Based on the detailed and compact thermal models, it is clearly seen that SOP thermal requirements can only be met with immersion cooling. The low performance of the today's available forced air cooling technologies, or low performance single phase direct liquid cooling, can not satisfy the cooling needs of advanced SOP systems. As given in Tables V through XIV, the maximum chip temperature can be maintained below the allowable level of 95 °C using phase change heat transfer.

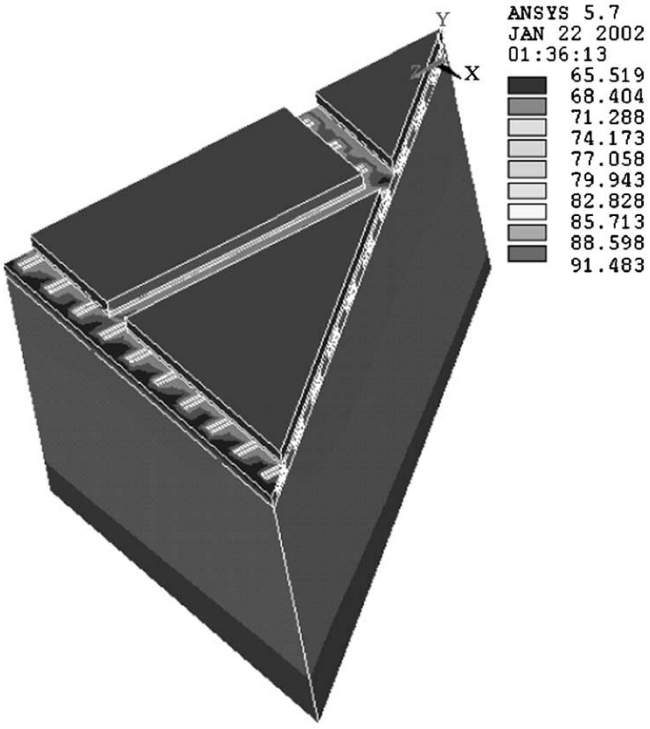

Fig. 19. Temperature profile of detailed model.

Nucleate boiling or spray cooling might be a candidate solution for successful thermal management.

V. IMMERSION COOLING FOR SOP PACKAGES

When chip heat fluxes approach or exceed 10 W/cm^2, it was mentioned that attention must be turned to nonconventional cooling techniques. Direct immersion cooling using dielectric liquids is a leading candidate for thermal management of SOP systems. The high dielectric strength and low dielectric constant of these liquids, as well as their chemical inertness, make

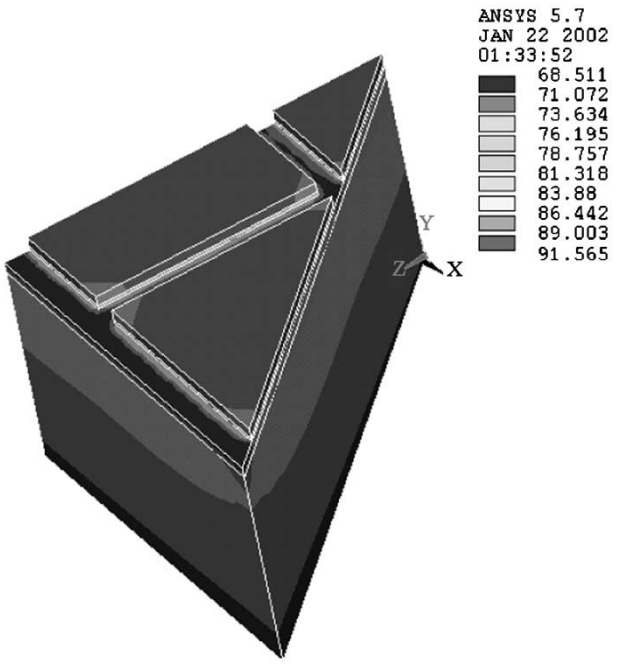

Fig. 20. Temperature profile of effective model.

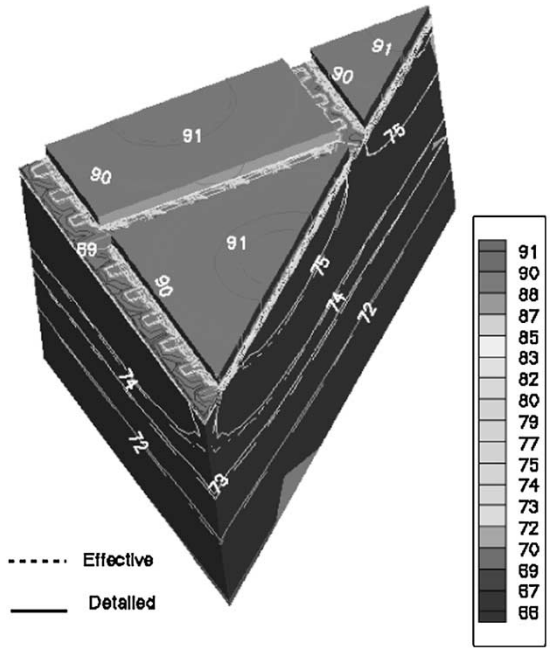

Fig. 21. Isotherms for both detailed and compact models.

it possible to immerse most electronic components directly in these fluorochemical fluids and thus remove component heat fluxes substantially in excess of 10 W/cm^2 with saturated pool boiling at the temperature differences typically less than 20 °C. Single phase immersion cooling, employing natural convection heat transfer, can also offer significant advantages, and serves to bridge the gap between direct air cooling and cold plate technology.

The primary candidate immersion cooling liquids are the perfluorocarbons. These highly wetting liquids are nontoxic, chemically inert to the packaging materials, and posses high dielectric strengths. They also have relatively low critical pressures, thermal conductivity and specific heats, and very large air solubility (20–25 times more than water). The fluorocarbon liquid FC-72 has been successfully used for single phase forced convection cooling of chips in the Cray-2 supercomputer (Danielsen, [12]). Moreover, another perfluorocarbon FC-77 has been used for jet impingement cooling of chips dissipating nearly 90 W/cm^2 in the SS-1 supercomputer (Ing. *et al.* [18]). Due to the relatively poor thermal properties of the fluorocarbons, extremely large flow velocities (about 10 m/s) are necessary to generate single phase heat transfer coefficients to cool high heat flux chips (Jiji and Dagan, [20]).

A passive immersion cooling system with nucleate pool boiling on the chip surface can provide high heat transfer coefficients within a 10–20 °C range, and eliminate the need for the expensive hardware and pumping power associated with single phase cooling designs. However, the departure from nucleate boiling, or Critical Heat Flux (i.e., CHF), places an upper limit on this highly efficient heat transfer mechanism. The CHF condition is associated with the formation of an insulating film of vapor on the heated surface leading to an increase in the surface temperature. CHF is associated with the formation of an insulating layer of vapor, which covers the entire heater surface. This results in a large increase in the heater surface temperature (about 1100°C for water, 150 K for FC-72). Consequently CHF is sometimes called the "burnout heat flux," and must be avoided in all practical boiling applications. Numerous experimental and theoretical studies, as reviewed in (Bar-Cohen *et al.* [7]), have established that fluid properties such as, density, latent heat of evaporation, temperature, specific heat, and heater properties such as, thickness, density, specific heat, thermal conductivity and surface quality can all affect the CHF. The composite CHF correlation (Bar-Cohen *et al.* [7]) has been compared with the experimental measurements of CHF for over 300 data points by Arik and Bar-Cohen [7]. It was observed that the CHF can be predicted within a 25% uncertainty for a wide range of data points. However, it was able to provide results within 8%, if attention was limited to a single chip package.

Spray cooling due to phase change is capable of removing high heat fluxes from surfaces with low superheat. Therefore, Evaporative spray cooling has been long identified as a technology that can be used to manage power densities exceeding 200 W/cm^2. A large number of experiments were performed by many researchers in order to understand nucleate boiling heat transfer and CHF for full cone sprays using single and multiple nozzles. However, limitations in the controllability of individual spray droplets have generally prevented the use in applications. Mudawar and Valentine [23] conducted an experimental study of spray cooling to determine local quenching characteristics for various regimes of a water spray boiling curve. It was found that the volumetric flux had a dominant effect on heat transfer compared to other hydrodynamic properties of the spray. Evaporative spray cooling has been presented as high as 1300 W/cm^2 for uniform heat sources with water and 300 W/cm^2 using dielectric fluids (Morgan *et al.*, [22]). Chang *et al.* [10] used FC-72 and FC-87, to spray cool a multichip module dissipating a uniform heat flux of 90 W/cm^2 and 60 W/cm^2, respectively. Pais *et*

TABLE X
MAXIMUM CHIP TEMPERATURE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	539 532	445 443	407 408	406 406	405 405	404 404	Air Jet Impingement
2000	127 126	117 117	105 105	104 104	103 103	103 102	FC Nucleate Boiling
3000	106 105	100 100	91 92	91 91	91 90	90 90	Spray Cooling

TABLE XI
AVERAGE CHIP TEMPERATURE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	521 522	438 438	406 406	405 405	404 404	403 402	Air Jet Impingement
2000	123 123	114 114	103 103	103 102	102 102	101 101	FC Nucleate Boiling
3000	103 103	98 98	90 90	89 89	89 89	89 89	Spray Cooling

TABLE XII
AVERAGE UNDER-FILL TEMPERATURE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	511 518	429 434	398 402	397 400	396 400	395 398	Air Jet Impingement
1000	173 177	151 155	133 136	132 135	131 134	130 133	FC Forced Convection
2000	118 121	109 112	97 100	97 99	96 99	95 98	FC Nucleate Boiling
3000	99 101	94 96	85 87	84 87	84 86	83 86	Spray Cooling

TABLE XIII
AVERAGE INTERCONNECT LAYER TEMPERATURE

k_{sub} / h	1	5	50	75	100	300	Remarks
200	498 498	417 419	388 390	386 388	386 388	384 387	Air Jet Impingement
2000	113 111	103 102	89 91	88 90	88 89	87 89	FC Nucleate Boiling
3000	94 92	88 88	78 79	77 79	77 78	76 77	Spray Cooling

al. [26] used water to spray over a laser diode surface, and the reported heat fluxes were exceeding 416 W/cm^2. With water as the working fluid, a spray cooling heat flux of 1000 W/cm^2 has been presented by Yang *et al.* [29].

In recent years, the spray cooling technology gained even more attention for high flux electronics cooling needs. Heffington *et al.* [16], have used vibration-induced droplet atomization to generate pseudo-random droplet ejection of water. The resulting spray pattern is generally uniform in nature and is directed toward a single heat source. Heat fluxes over 100 W/cm^2 over a uniform surface was reported. Pautsch [27] presented of the spray cooling thermal management scheme for high flux CRAY SV2 supercomputer system utilizing using FC-72. Lin and Ponappan [21] presented the results of experiments in FC-87, FC-72, methanol and water. Thermal performance data for the multinozzle spray cooling in the confined and closed system were given at various operating temperatures, nozzle pressure drops (0.7–3.1 Bar) and heat fluxes were found to be 90 W/cm^2 with PFCs, 490 W/cm^2, and 500 W/cm^2 with methanol and water, respectively. Bash *et al.* [9] demonstrated the utilization of thermal inkjet technology to spray over a chip source with nonuniform power density. The independent control of micro-nozzles in an array makes the technology well suited to nonuniform heat removal. Application of the technology to the thermal management of electronics has been described in this report and it has been experimentally shown that heat fluxes up to 270 W/cm^2 can be dissipated with water while maintaining a high coefficient of performance.

Although substantially high fluxes can be achieved with spray cooling, design of a successful spray cooling scheme is nontrivial. The flow rates are generally based on the maximum power density and excess liquid is accumulated in the system.

TABLE XIV
AVERAGE SUBSTRATE TEMPERATURE

k_{sub} h	1	5	50	75	100	300	Remarks
200	465 439	405 397	383 383	382 382	382 382	381 381	Air Jet Impingement
2000	106 100	97 94	86 86	85 85	85 85	84 84	FC Nucleate Boiling
3000	89 85	84 81	75 75	74 74	74 74	73 73	Spray Cooling

TABLE XV
FLUID PROPERTIES AT ATMOSPHERIC PRESSURE BOILING POINT (ARIK, [3])

Property	FC-40	FC-72	HFE-7100	HFE-7200	R-113	Water
T_{sat} (°C)	156.0	56.0	61.0	76.0	48	100.0
ρ_f (kg/m^3)	1870.0	1623.0	1500.0	1430.0	1511	957.8
ρ_v (kg/m^3)	25.0	12.7	9.6	9.26	7.4	0.5956
μ_f (mN m/s^2)	3.54	0.457	0.61	0.61	0.503	0.279
C_{pf} (J/kg-K)	-	1097.8	1180.0	1210.0	979	4217.0
k_f (W/m-K)	-	0.052	-	-	0.702	0.68
h_{fv} (kJ/kg)	711.6	84.97	125.6	122.6	146.8	2257.0
σ_f (N/m)	0.016	0.0084	0.014	0.014	0.0147	0.0589
P_{cr} (kPa)	1176.0	1840.0	-	-	-	22100.0

Pumping needs, fluid type and amount are defined for the maximum power dissipation. Since system has rotating parts, the reliability of the system is significantly reduced. The choice of the dielectric fluid type and amount is another constraint. A hermetic sealing, as well as material compatibility are vital to have a reliable design. Another design factor is the temperature distribution on the surface. High flux electronics usually have nonuniform temperature distributions on the surface. When a uniform spray pattern is applied to such an electronics structure, different heat transfer modes on the surface might occur. Coolant might build up in the low-power dissipation places. This can result in pool boiling heat transfer. While it is expected to have high spray cooling heat transfer, pool boiling CHF might take place.

VI. CLOSING REMARKS

The relentless improvements in semiconductor technology have continued to lower the cost of electronic systems and to create a nearly endless succession of new products. Successful exploitation of future semiconductor technology will, however, require significant improvements in packaging density and dramatic reductions in packaging costs. In response to these needs, the Packaging Research Center (PRC) at the Georgia Institute of Technology, Atlanta, has undertaken the development of the System on Package (SOP) technology, capable of combining RF and optoelectronic devices with logic and memory circuits in a single module. Fig. 7 shows the GIT Packaging Research Center SOP and Table V shows the PRC technology roadmap. It may be seen that SOP is expected to dissipate l0 W/cm^2 in Phase 1, 20 W/cm^2 in Phase 2, and up to 100 W/cm^2 in Phase 3. Silicon efficiency defined as total chip area over total PCB area, will go up from 25% to 85% in a decade (PRC Report, [25]) which that means less PCB area will be available for heat spreading and heat removal.

Air cooling is always the first choice in the thermal management of electronic systems. However, the thermophysical characteristics of air limit its utility. The maximum heat transfer coefficient in natural convection air cooling can be expected to be about 10 W/m^2-K, including the heat loss due to radiation. In forced convection air cooling the heat transfer coefficient can approach 60–70 W/m^2-K with a blower that is directing air to the chip with very high velocity. However, natural convection liquid cooling with perfluorocarbons can provide five times higher heat transfer coefficients as forced convection with air. Passive immersion liquid cooling can also provide other advantages, resulting from the elimination of blowers or pumps and the consequent elimination of additional capital investments, maintenance problems, and acoustic noise (a major problem with air cooling systems). While novel techniques may make it feasible to rely on air cooling to meet the requirements of the Phase 1 SOP, this situation is unlikely to persist to Phase 3, when aggressive cooling will be needed to deal with this extremely high heat flux configuration.

Alternatively, direct liquid cooling could be used to provide effective thermal management across the entire envelope of the SOP design. In Phase I this could be accomplished by use of

liquid natural convection. High velocity forced convection or pool boiling could provide adequate thermal management for Phase 2. Relatively high-velocity forced convection, low velocity flow boiling, or enhanced pool boiling CHF would be required to deal with the thermal challenge posed by Phase 3 requirements.

Previous sections have explored the CHF phenomena, parametric sensitivities, and passive enhancement techniques, as well as the use of a recent correlation for this important inflection point in the pool boiling curve. Based on our current understanding and correlation of enhanced CHF, it appears possible to reach a CHF of nearly 45 W/cm^2, using elevated pressure and subcooling, along with a dilute mixture of a high boiling point fluorocarbon. Moreover, when a microporous coating is applied to the surface of the bare chip, a further increase about 40 to 50% can be anticipated [3]. It would thus appear that pool boiling heat transfer, taking advantage of passive enhancements to reach a CHF value of some 60 W/cm^2, could be used to provide direct liquid cooling of the Phase 3 SOP design. Additional enhancement techniques, currently under study in the Laboratory, as well as a hybrid pool-flow boiling approach could be used to extend the thermal management envelope to the highest chip flux considered, i.e., 100 W/cm^2.

VII. Summary and Conclusion

Air has always been preferred as a coolant for the thermal management of electronic components, although its thermopysical properties are very poor in comparison with liquids. Maximum heat transfer coefficient with forced air cooling, by utilizing very high velocities, is about 5 times less than natural convection liquid cooling that does not require any pumping power. The use of direct liquid cooling, employing immersion of the components in an inert, nontoxic, high dielectric strength perfluorocarbons can provide much better heat removal process. When the desired heat fluxes are very high, the upper limit of liquid cooling with phase change, CHF, must be addressed. As a result of the experimental findings, it has been shown that a CHF of nearly 60 W/cm^2, using elevated pressure and subcooling, along with a dilute mixture of a high boiling point fluorocarbon was achieved on plain heater surfaces. In addition, applying a micro porous coating to the surface of the chip has been shown that CHF can be increased by 50%. Therefore, the judicious combinations of these known enhancement techniques would appear to promise CHF values approaching 100 W/cm^2, the target value for the SOP. Spray cooling can also achieve over 100 W/cm^2 heat fluxes. However, moving parts and selected spraying requirements might be major hurdles for thermal design engineers to implement this technology.

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